

Modeling and Prototyping of MEMS-Based Cantilever Resonators

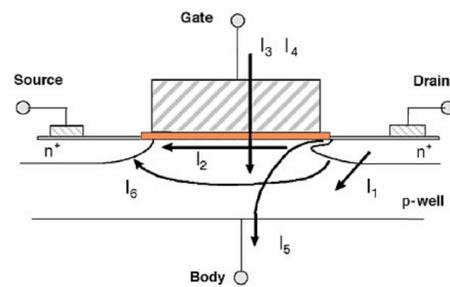
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1. Problem Statement

The objectives of the project are to model a cantilever Metallic Oxide Semiconductor Field Effect Transistor (MOSFET) in the micro/nano scale with an on/off voltage less than 1 V that is capable of frequencies greater than 1 GHz by optimizing the cantilever materials and geometry and also build a mock-up prototype.



I_1 is Reverse-bias pn junction leakage
 I_2 is Subthreshold leakage
 I_3 is Oxide tunneling current
 I_4 is Gate current due to hot-carrier injection
 I_5 is Gate induced drain leakage
 I_6 is channel punch-through current

Figure 1: NMOS, Showing the ON, Transition and OFF State Leakage Currents.

2. Background

2.1 Subthreshold Leakage Current Effect

- MOSFET turns off, output voltage is high.
- Current flowing in the channel due to V_{DD} (drain voltage) potential of V_{DS} (drain-source voltage).
- High voltage which is mainly affected by I_{SUB} (Subthreshold leakage current) the largest of leakage currents.
- Threshold leakage increases with temperature.

2.2 Figure below show Subthreshold Effect on CMOS

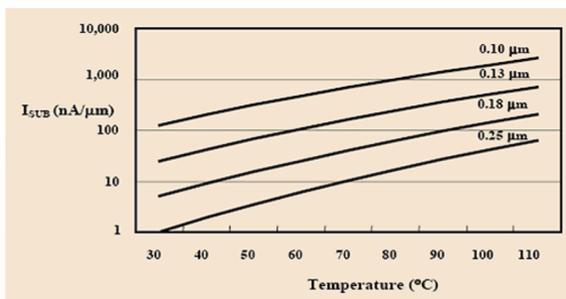


Figure 2: I_{SUB} ($V_{GB} - 0$) trend as a function of temperature. Courtesy of Vivek De, Intel.

2.3 Leakage power of 0.1 um die shows increasing power consumption due to increasing temperature

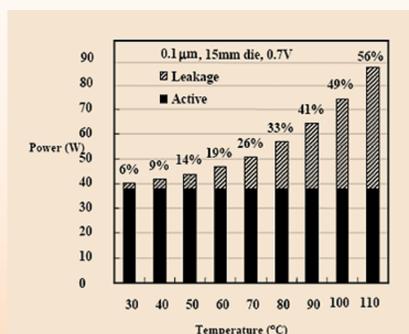


Figure 3: Power consumption of a die as a function of temperature. Courtesy of Vivek De, Intel.

3. CMOS Problem

Power Consumption: As size decreases, CMOS conducts current in “off” mode. Typically, the power dissipation due to current leakages of ICs below the size of 100 nm is half total power dissipation. This effect causes poor performance and shorten the battery life.

4. Option Selection

The final model was selected out of three main design models: Separate Source, Separate Gate, and Separate Drain models.

5 main factors were considered for choosing the model and each factor was weighted as shown in Figure 5.

Separate Source Model gained the highest score of 50 points so that was selected.

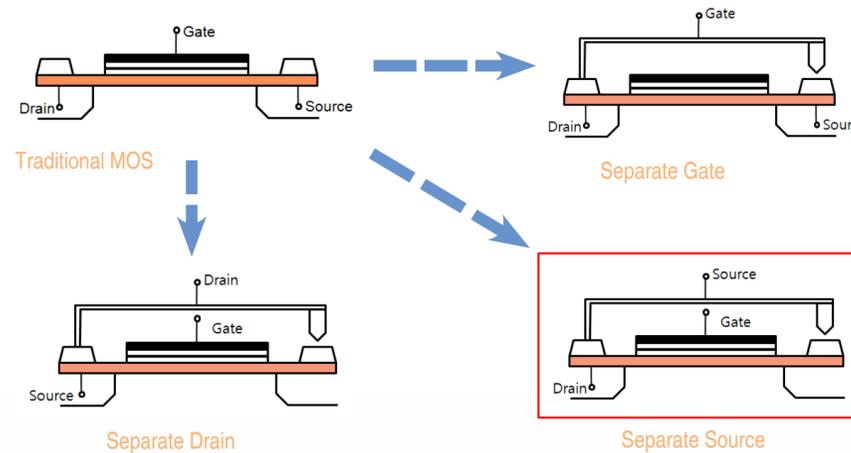


Figure 4: The design models considered. The design (Separate Source) with the red outline was the design selected based on the option selection chart.

4.1 Option Selection Chart

Metric (PDS)	Criteria	Concept Weight	Separate Gate	Separate Source	Separate Drain
2	Gate to Source Leakage Current	20	1	1	0
2	Drain to Source Leakage Current	20	0	1	0
2	Source to Substrate Leakage Current	10	0	1	0
4,11,16	Cost	10	1	0	0
4,11,14	Build Time	5	1	0	0
	Total	65	35	50	0
	Rank		2	1	3

Figure 5: The option selection chart is based 5 factors; the Gate to Source leakage current, Drain to Source Leakage current, Source to Substrate leakage, Cost and Build time. The design with the highest point yielded 50 points, i.e. Separate Source.

5. Modeling

The merit function maximizing the ratio of the Natural Frequency to the Pull-in Voltage requires a beam with a small length, width, and height. This implies a beam with any combination of Pull-in Voltage lower than a threshold and a Natural Frequency higher than a threshold is possible. The question becomes: “Is it possible to make a cantilever small enough to satisfy the constraints.”

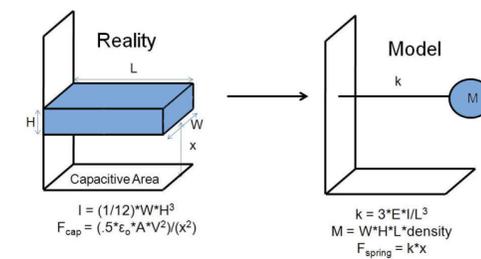


Figure 6: Model Realization. How our model compares with the reality of the situation.

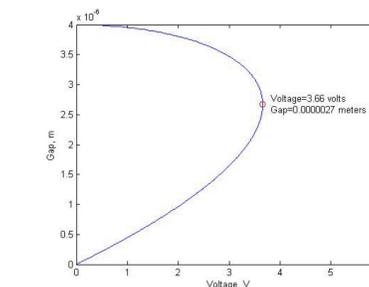


Figure 7: Pull-in Voltage Visualization.

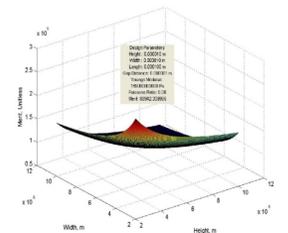


Figure 8: Merit Function Relating Natural Frequency and Pull-in Voltage (Merit=Natural Frequency/Pull-in Voltage).

6. Prototype

A mock-up prototype has been built to illustrate the effect of the cantilever based FET.

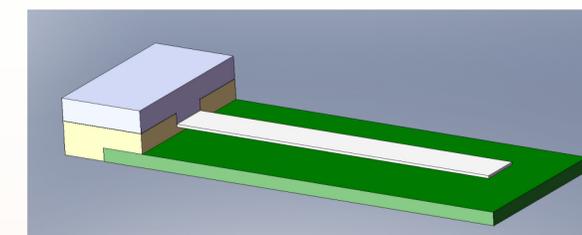


Figure 9: Prototype built and the dimensions used.

7. Conclusion

Project objectives have been met with the modeling and prototyping of a cantilever based resonator. With the model and design selected, we are able to eradicate a bigger chunk of current leakage problem associated with the traditional CMOS.

8. Acknowledgement

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