Review of 6T SRAM Cell

Ding-Ming Kwai
Intellectual Property Library Company
June 3, 2005
Why 6T SRAM Cell

- Embedded memory
  - Easy to implement in generic CMOS process
  - Easy to design as logic circuit
  - Easy to test by finite-state machine

- Compilable design
  - Fixed cell size to allow us dedicating in peripheral circuit design
  - Synchronous interface since 0.35µm generation simplifies the design
  - A larger number of instances required
Outline

- **6T cell and its variants** – First we generalize and then we derive
- **Peripheral circuits** – Utilization is the key
- **Cell layout** – To be symmetric or to be asymmetric: that is the question
- **Performance indices** – To judge is human
- **Concluding remarks** – It does not end here
8T SRAM Cell

Making it completely complementary

- Regenerative circuit for storing a single bit: two equal-sized inverters
- Access device to transfer the bit: two equal-sized transmission gates ⇒ pass transistors
What Have Been Invented

NEC, 1969

NEC, 1975

NEC, 1995
What Have Been Invented (Continued)

NEC, 1998

IBM, 1970
GE, 1985

IBM, 1976
MOSTEK, 1981
“The World’s Smallest” Myth

Cell size as a competitive edge

Reach a consensus at last!

Tradeoffs to Be Made

- Small but slow ⇔ large but fast: area vs. speed (read current and write voltage)
- Small but hot ⇔ large but cold: area vs. leakage power (standby current)
- Small but unstable ⇔ large but stable: area vs. stability (static noise margin)
- Small but low-yield ⇔ large but high-yield: area vs. manufacturability
- Small but expensive ⇔ large but cheap: area vs. cost (masking and process steps)
Outline

- **6T cell and its variants** – First we generalize and then we derive
- **Peripheral circuits** – Utilization is the key
- **Cell layout** – To be symmetric or to be asymmetric: that is the question
- **Performance indices** – To judge is human
- **Concluding remarks** – It does not end here
Utilization Is the Key

0.18µm single-port compiler generated instances with peripheral circuits minimized for layout area

![Graph showing area saving percentage vs. capacity (log_2(N))](image)

- Divided Bit-Line Drive
- Extra Column Mux

Area Saving (%) vs. Capacity (log_2(N))
What Is Column Mux and Why It Is Important

\[ C = n_R \cdot n_C = w_W \cdot w_D \]

\[ n_R = \frac{w_D}{M}, \quad n_C = w_W \cdot M \]
P&R Can Easily Destroy It

0.18µm single-port compiler generated instances added with redundant power/ground rings

Utilization (%) vs. Capacity ($\log_2(N)$) for different ring widths:
- 0µm
- 10µm
- 25µm
- 40µm

SRAM
Outline

- 6T cell and its variants – First we generalize and then we derive
- Peripheral circuits – Utilization is the key
- Cell layout – To be symmetric or to be asymmetric: that is the question
- Performance indices – To judge is human
- Concluding remarks – It does not end here
How They Are Drawn
(TSMC 0.18µm Symmetric Example)

How They Are Drawn
(TSMC 0.13μm Asymmetric Example)
How They Are Drawn

(Intel 0.18µm Symmetric Example)

Asymmetry in cross-coupled inverters can degrade cell stability by **100X** [may be exaggerated]

---

How They Are on Silicon

Symmetric and Asymmetric Examples

Poly and Diffusion for Devices

0.13μm
Intel 1.22 × 1.64 μm²

0.13μm
IBM 1.2 × 1.7 μm²

90nm
Fujitsu 0.9 × 1.1 μm²

How They Are on Silicon
Symmetric and Asymmetric Examples

Metal-1 as Local Interconnect

0.13µm
Intel 1.22 × 1.64 µm²

0.13µm
IBM 1.2 × 1.7 µm²

90nm
Fujitsu 0.9 × 1.1 µm²

How They Are Drawn

IBM 0.13µm Example for ULP SRAM

Disadvantages Related to Conventional Cell Layout

- Complicated irregular patterns involving corner rounding
  - Simplified rectangular pattern
- Different orientation for access NMOS transistors
  - Same orientation for all transistors
- Pushed spacing rules for metal routing
  - Nominal spacing rules for metal routing
Variations by Inverter Layout

A Reveal Close to Success


It turns out to be very useful in 90nm and below process technologies.
Can We Draw the Polygons in Another Way?

**Metal-Layer Assignment for Routing**

<table>
<thead>
<tr>
<th></th>
<th>Symmetric</th>
<th>Asymmetric</th>
<th>Symmetric</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>WL (H)</strong></td>
<td>M3</td>
<td>M2</td>
<td>M2</td>
</tr>
<tr>
<td><strong>BL (V)</strong></td>
<td>M2</td>
<td>M3</td>
<td>M3</td>
</tr>
<tr>
<td><strong>VSS (V)</strong></td>
<td>M2</td>
<td>M3</td>
<td>M3</td>
</tr>
</tbody>
</table>

Vertical VSS lines parallel to bit lines are required in the memory array.
Can We Draw the Polygons in Another Way?

SRAM Cell Aspect Ratio

Technology Node

- 0.25μm
- 0.18μm
- 0.13μm
- 90nm
- 65nm

SRAM Cell Aspect Ratio

> 1.2

< 0.5
An Animation to Show Layout
Changes to Rectangular Patterns

Original Symmetric Layout
Photo Demonstrations at 65nm Technology Node

It seems that the layout style will pervade!

TI $0.46 \times 1.06 \ \mu m^2$
$0.49 \ \mu m^2$

IBM $0.41 \times 1.25 \ \mu m^2$
$0.51 \ \mu m^2$

Intel $0.46 \times 1.24 \ \mu m^2$
$0.57 \ \mu m^2$

Disadvantages Related to Regular Pattern Cell Layout

- Longer and narrower wells
  - Induce forward body bias
  - Reduce static noise margin
  - Require higher strapping frequency
  - Lower array utilization

- More irredundant contacts and via holes
  - 10 contacts/cell ⇔ 8.5 contacts/cell
  - 3.5 via-1 holes/cell ⇔ 2 via-1 holes/cell
  - 2.5 via-2 holes/cell ⇔ 0 via-2 holes/cell
Outline

- **6T cell and its variants** – First we generalize and then we derive
- **Peripheral circuits** – Utilization is the key
- **Cell layout** – To be symmetric or to be asymmetric: that is the question
- **Performance indices** – To judge is human
- **Concluding remarks** – It does not end here
Cell (Read) Current

Bit-Line Discharge Current

\[ \Delta V_{BL} = I_{cell} \cdot \Delta t/C_{BL} \]

- **A = ‘0’ and B = ‘1’**
  - Current: \( I_{cell0} \)
  - Discharge current: \( I_{cell} \)

- **A = ‘1’ and B = ‘0’**
  - Current: \( I_{cell1} \)

- BitLine Discharge Current

- Voltage Change in BitLine

\[ \Delta V_{BL} = \frac{I_{cell}}{C_{BL}} \Delta t \]
Bounds on Cell Current
where Cell Ratio $\gamma$ comes in

$$
\gamma = \frac{I_{SD}}{I_{SA}} = \frac{W_D \cdot L_A}{L_D \cdot W_A}
$$

$$
I_{cell} < I_{SA}
$$

$$
I_{cell} > \frac{I_{SA} \cdot I_{SD}}{I_{SA} + I_{SD}} = \frac{\gamma \cdot I_{SA}}{\gamma + 1}
$$

$$
I_{cell} < \frac{I_{SD}}{\gamma}
$$

$$
I_{cell} > \frac{I_{SD}}{\gamma + 1}
$$
Saturation Current Monitor Is Not Good Enough

0.18µm SRAM Cell

\[ ISD = \gamma \cdot I_{SA} \]

\[ ISD \left( \frac{\gamma + 1}{\gamma} \right) \]

Cell Current (µA) vs. VDD (V)

1.2 1.3 1.4 1.5 1.6 1.7 1.8 1.9 2.0

0 25 50 75 100 125 150
On-Chip Measurement of Cell Current
Location Dependence of Cell Current

- Cells are divided into two groups by their discharge paths (half cells) being next to a strap of a sub-array or not.
- Boundary cells tend to have a smaller mean and a larger standard deviation.

<table>
<thead>
<tr>
<th></th>
<th>Boundary</th>
<th>Interior</th>
</tr>
</thead>
<tbody>
<tr>
<td>Median</td>
<td>90.68 µA</td>
<td>91.11 µA</td>
</tr>
<tr>
<td>Average</td>
<td>90.75 µA</td>
<td>91.17 µA</td>
</tr>
<tr>
<td>Std Dev</td>
<td>1.77 µA</td>
<td>1.68 µA</td>
</tr>
</tbody>
</table>

Cell Current (µA)
Static Noise Margin (SNM)

Every cell has to demonstrate

- Static noise is the DC disturbance present in logic gates
- The worst case occurs when the static noise is adversely present in all logic gates in the same way
- It is the most important parameter of an SRAM cell

Shift of Meta-stable Point

Maximum Squares in Butterfly Curves
**Static Noise Margin as a Function of Supply Voltages**

![3D Graph showing SNM (V) as a function of CVDD and PVDD](image)

WL = BL = \overline{BL} = PVDD

Static Noise Margin as a Function of Precharge Voltages


 WL = VDD, BL = \overline{BL}
Static Noise Margin as a Function of Bit-Line Voltages

\[ \text{SNM} (V) = C_{VDD} - C_{VSS} \]

\[ WL = CVDD = VDD \]
Static Noise Margin as a Function of Source Voltages

Outline

- **6T cell and its variants** – First we generalize and then we derive
- **Peripheral circuits** – Utilization is the key
- **Cell layout** – To be symmetric or to be asymmetric: that is the question
- **Performance indices** – To judge is human
- **Concluding remarks** – It does not end here
What Revive 6T SRAM Cell

- Panel display driver/controller
  - Large wafer quantity that foundries cannot refuse
  - Shrinking pad pitch that cell size becomes an issue
  - Lag behind the most advanced process at least three generations
  - Power, either static or dynamic, is the concern
Challenges in the Future

- To many simulation works, too few measurement results
- Not only to show it functional, but also to prove it manufacturable
- To invent a new cell is costly, it will be a pity to serve only one purpose
- There are still some things we do not know well (e.g., substrate noise)